CLAIMS

What is claimed is:

1. A Semiconductor device comprising:

- a semiconductor substrate,
- an insulating layer on top of said substrate,
- a lateral field effect transistor comprising a drain region and a source region arranged in said substrate and a gate arranged above said substrate within said insulating layer,
- a drain runner arranged on top of the insulator layer above said drain region,
- a source runner arranged on top of the insulator layer above said source region,
- a gate runner arranged on top of the insulator layer outside an area defined by said drain runner and said source runner,
- a first coupling structure comprising a via for coupling said drain runner with said drain region, and
- a second coupling structure comprising a via for coupling said source runner with said source region.

2. The Semiconductor device as claimed in Claim 1, wherein said first and second coupling structure further comprise barrier metal layers arranged at the bottom of said via.

3. The Semiconductor device as claimed in Claim 1, wherein said first and second coupling structure further comprise barrier metal layers arranged at the top of said via.

4. The Semiconductor device as claimed in Claim 2, wherein said bottom barrier metal layer has a cross-sectional profile of a saucer around said via.

5. The Semiconductor device as claimed in Claim 4, wherein the bottom barrier metal layer comprises side walls that enclose said via.

6. The Semiconductor device as claimed in Claim 4, wherein the bottom barrier metal layer comprises side walls that are spaced apart from said via.

7. The Semiconductor device as claimed in Claim 2, wherein the bottom barrier metal layer consists of Titanium-Titanium nitride.

8. The Semiconductor device as claimed in Claim 3, wherein the top barrier metal layer consists of Titanium-Platinum.

9. The Semiconductor device as claimed in Claim 1, wherein the via comprises tungsten.

10. The Semiconductor device as claimed in Claim 1, further comprising a sinker structure that reaches from the top to the bottom of said substrate.

11. The Semiconductor device as claimed in Claim 10, further comprising a backside metal layer arranged on the bottom surface of said substrate.

12. The Semiconductor device as claimed in Claim 1, further comprising a well structure surrounding said source region.

13. The Semiconductor device as claimed in Claim 1, further comprising a substrate via within said source area located under said source runner reaching from the top of said substrate to the bottom of said substrate.

14. The Semiconductor device as claimed in Claim 13, wherein said substrate via is filled with Tungsten or copper.

15. The Semiconductor device as claimed in Claim 14, further comprising a backside metal layer arranged on the bottom surface of said substrate and a barrier metal layer between said Tungsten or copper filled substrate via and said backside metal layer.

16. The Semiconductor device as claimed in Claim 14, further comprising a well structure surrounding said source region.

17. The Semiconductor device as claimed in Claim 2, wherein said barrier metal layer between the source region and the via is extended to form a field plate in such a way that it covers at least partly said gate.

18. The Semiconductor device as claimed in Claim 17, wherein the field plate covers part of the top surface of the gate and the side of the gate facing the drain runner.

19. The Semiconductor device as claimed in Claim 18, wherein the field plate is coupled with the barrier metal layer at a single location.

20. The Semiconductor device as claimed in Claim 17, wherein the field plate extends from the barrier metal layer to cover part of the left, top and right side of the gate.

21. The Semiconductor device as claimed in Claim 1, wherein the first coupling structure comprises a plurality of vias.

22. The Semiconductor device as claimed in Claim 1, wherein the second coupling structure comprises a plurality of vias.

23. The Semiconductor device as claimed in Claim 17, wherein the field plate comprises at least one cut out area.

24. The Semiconductor device as claimed in Claim 1, wherein the substrate comprises a p+ substrate and p- epitaxial layer.

25. A method for manufacturing a semiconductor device comprising the steps of:

- providing a substrate comprising a lateral field effect transistor comprising a drain region and a source region arranged in said substrate,
- depositing an first insulating layer on top of said substrate,
- forming at least one window structure on top of said drain and source region, respectively,
- depositing a barrier metal layer within said window structures,
- depositing a second insulating layer on top of said substrate,
- forming vias within said insulating layer on top of said barrier metal layer,
- filling said vias with metal,
- planarizing the surface,
- depositing a runner structure over said vias on said surface.

26. The method as claimed in Claim 25, further comprising the step of depositing a second barrier metal layer on top of said via before depositing said runner.

27. The method as claimed in Claim 25, wherein said barrier metal layer has the cross-sectional profile of a saucer by overlapping the edges of said window.

28. The method as claimed in Claim 25, wherein the barrier metal layer consists of Titanium-Titanium nitride.

29. The method as claimed in Claim 26, wherein the second barrier metal layer consists of Titanium-Platinum.

30. The method as claimed in Claim 25, wherein the via is filled with tungsten.

31. The method as claimed in Claim 25, further comprising the step of forming a substrate via within said source area reaching from the top of said substrate to the bottom of said substrate before depositing said barrier metal layer.

32. The method as claimed in Claim 31, wherein said substrate via is filled with copper.

33. The method as claimed in Claim 25, wherein the barrier metal layer is extended to cover at least partly said gate formed within the insulating layer deposited on said barrier metal layer.

34. The method as claimed in Claim 25, further comprising the step of implanting a sinker which reaches from the surface of the substrate located at the source barrier metal layer to the bottom of the substrate.

35. The method as claimed in Claim 25, wherein the substrate comprises a p+ substrate and p- epitaxial layer.

36. A Semiconductor device comprising:

- a semiconductor substrate,
- an insulator layer on top of said substrate,
- a lateral field effect transistor comprising a drain region and a source region arranged in said substrate and a gate arranged above said substrate within said insulator layer,
- a drain runner arranged in said insulator layer above said drain region,
- a source runner arranged in said insulator layer above said source region,
- a gate runner arranged in said insulator layer outside an area defined by said drain runner and said source runner,
- a first coupling structure comprising a via for coupling said drain runner with said drain region,
- a second coupling structure comprising a via for coupling said source runner with said source region,
- wherein said first and second coupling structure further comprise barrier metal layers arranged at the top and the bottom of said via,
- a sinker structure that reaches from the top to the bottom of said substrate, and
- a backside metal layer arranged on the bottom surface of said substrate.

37. The Semiconductor device as claimed in Claim 36, wherein said barrier metal layer between the source region and the via is extended to form a field plate in such a way that it covers at least partly said gate.

38. The Semiconductor device as claimed in Claim 36, wherein the substrate comprises a p+ substrate and p- epitaxial layer.

39. A Semiconductor device comprising:

- a semiconductor substrate,
- an insulator layer on top of said substrate,
- a lateral field effect transistor comprising a drain region and a source region arranged in said substrate and a gate arranged above said substrate within said insulator layer,
- a drain runner arranged in said insulator layer above said drain region,
- a source runner arranged in said insulator layer above said source region,
- a gate runner arranged in said insulator layer outside an area defined by said drain runner and said source runner,
- a first coupling structure comprising a via for coupling said drain runner with said drain region,
- a second coupling structure comprising a via for coupling said source runner with said source region,
- wherein said first and second coupling structure further comprise barrier metal layers arranged at the top and the bottom of said via,
- a substrate via filled with metal within said source area located under said source runner reaching from the top of said substrate to the bottom of said substrate, and
- a backside metal layer arranged on the bottom surface of said substrate and a barrier metal layer between said filled substrate via and said backside metal layer.

40. The Semiconductor device as claimed in Claim 39, wherein said barrier metal layer between the source region and the via is extended to form a field plate in such a way that it covers at least partly said gate.

41. The Semiconductor device as claimed in Claim 39, wherein the substrate comprises a p+ substrate and p- epitaxial layer.

42. A Semiconductor device comprising:

- a semiconductor substrate,
- an insulator layer on top of said substrate,
- a backside metal layer,
- a lateral field effect transistor comprising a drain region and a source region arranged in said substrate and a gate arranged above said substrate within said insulator layer,
- a drain runner arranged in said insulator layer above said drain region,
- a source runner arranged in said insulator layer above said source region,
- a gate runner arranged in said insulator layer outside an area defined by said drain runner and said source runner,
- a first coupling structure comprising a via for coupling said drain runner with said drain region,
- a second coupling structure comprising a via for coupling said source runner with said backside metal layer.

43. The Semiconductor device as claimed in Claim 42, wherein said first and second coupling structure further comprise barrier metal layers arranged at the bottom of said via.

44. The Semiconductor device as claimed in Claim 42, wherein said first and second coupling structure further comprise barrier metal layers arranged at the top of said via.

45. The Semiconductor device as claimed in Claim 43, wherein the bottom barrier metal layer consists of Titanium-Titaniumnitride.

46. The Semiconductor device as claimed in Claim 42, wherein the via of the second coupling structure comprises an insulating side wall layer.

47. The Semiconductor device as claimed in Claim 42, wherein the via of the second coupling structure is filled with tungsten.

48. The Semiconductor device as claimed in Claim 47, wherein the via further includes a Tantalum-Tantalum nitride-copper seed layer covering the tungsten layer.

49. The Semiconductor device as claimed in Claim 48, wherein the via is filled with copper.

50. The Semiconductor device as claimed in Claim 42, further comprising a well structure surrounding said source region.

51. The Semiconductor device as claimed in Claim 42, further comprising a field plate that covers at least partly said gate.

52. The Semiconductor device as claimed in Claim 51, wherein the field plate covers part of the top surface of the gate and the side of the gate facing the drain runner.

53. The Semiconductor device as claimed in Claim 42, wherein the first coupling structure comprises a plurality of vias.

54. The Semiconductor device as claimed in Claim 43, wherein the second coupling structure comprises a plurality of vias.

55. The Semiconductor device as claimed in Claim 43, wherein the second coupling structure further comprises a source via for coupling said source runner with said source region.

56. The Semiconductor device as claimed in Claim 55, wherein said source via comprises barrier metal layers arranged at the top and the bottom of said source via.

57. The Semiconductor device as claimed in Claim 56, wherein said bottom barrier metal layer has a cross-sectional profile of a saucer around said via.

58. The Semiconductor device as claimed in Claim 56, wherein the top and bottom barrier metal layer consists of Titanium-Titaniumnitride.

59. The Semiconductor device as claimed in Claim 55, wherein the source via comprises tungsten.

60. The Semiconductor device as claimed in Claim 55, wherein the second coupling structure comprises a plurality of vias and source vias which are arranged in an alternative pattern.

61. The Semiconductor device as claimed in Claim 42, wherein the substrate comprises a p+ substrate and p- epitaxial layer.

62. A method for manufacturing a semiconductor device comprising the steps of:
- providing a substrate comprising a lateral field effect transistor comprising a drain region and a source region arranged in said substrate and a gate structure arranged in an insulating layer deposited on top of said substrate,
- performing a planarization process on top of said substrate,
- forming a hard mask on top of said substrate including at least one window structure on top of said drain and source region, respectively,
- etching at least one via through said window within said substrate,
- filling said vias with metal,
- forming a metal runner structure on top of said via,
- grinding the bottom surface of said substrate to expose the metal within said via.

63. The method as claimed in Claim 62, wherein the step of filling the via with metal comprises the steps of:
- depositing an insulation layer in said via,
- depositing a metal within said via.

64. The method as claimed in Claim 63, wherein the step of depositing an insulation layer includes the steps of:
- depositing undoped silicon glass in said via,
- sputtering and annealing said via with Titanium-Titanium nitride.

65. The method as claimed in Claim 63, wherein the step of depositing a metal includes the steps of:
- depositing tungsten in said via,
- sputtering via with a Tantalum-Tantalum nitride/ Copper layer,
- filling said via with copper.

66. The method as claimed in Claim 62, further comprising the step of depositing a barrier metal layer on top of said via before forming the metal runner.

67. The method as claimed in Claim 62, wherein after the step of filling the via with metal the top surface of said substrate is planarized by chemical mechanical polishing.

68. The method as claimed in Claim 62, further comprising the steps of depositing a barrier metal layer on the exposed metal of said via.

69. The method as claimed in Claim 62, further comprising the step of depositing a metal layer on the backside of the substrate.

70. The method as claimed in Claim 62, wherein the substrate comprises a p+ substrate and p- epitaxial layer.